COURSE INSTRUCTORS

STEVE HOOVER

Steve Hoover is the founder of Redwood EDA, a Massachusetts startup specializing in emerging digital logic modeling tools and methodology. He brings with him into this role a deep understanding of the complexities of high-performance IC design, having contributed to multiple generations of Alpha microprocessors at DEC and Compaq as well as Itanium and Xeon server projects and Omni-Path HPC network switch microarchitecture for Intel.

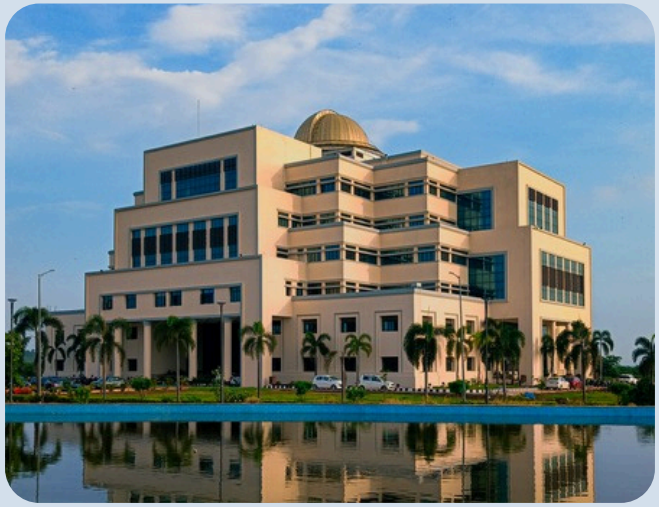
DR. SRINIVAS BOPPU

Dr. Srinivas Boppu is an Assistant Professor in the School of Electrical and Computer Sciences, IIT Bhubaneswar. His research interests include high-level synthesis, design of programmable hardware accelerators, and design automation for integrated circuits.

DR. AYAN PALCHAUDHURI

Dr. Ayan Palchaudhuri is an Assistant Professor in the School of Electrical and Computer Sciences at IIT Bhubaneswar. His research interests include VLSI architecture design for high performance computer arithmetic applications.

ABOUT IIT BHUBANESWAR



Indian Institute of Technology Bhubaneswar is established by the Government of India in 2008 under The Institutes of Technology Act 1961 with amendments up to 2012. IIT Bhubaneswar became an institute of national importance from 29th June 2012 with notification of amendment in the Institutes of Technology Act, 1961, by the Ministry of Education, (Department of Higher Education) Government of India published in the Gazette of India dated 2nd July 2012.

With a vision to attain global recognition through exceptional graduates and innovative research, IIT Bhubaneswar fosters a learning community that promotes interdisciplinary collaboration and encourages creativity, cognitive thinking, and entrepreneurship. The mission of the Institute includes nurturing a learning community based on mutual respect, interdisciplinary collaboration, innovation, flexible curricula, and strong industry-academia partnerships.

CONTACT

0091-674-7135752

srinivas@iitbbs.ac.in / ayan@iitbbs.ac.in

School of Electrical and Computer Sciences,
IIT Bhubaneswar, Odisha, India- 752050

A SHORT COURSE ON

Next-Generation Semiconductors: RISC-V, AI, and TL-Verilog

MOE Scheme on

Global Initiative on Academic Network

GIAN
GLOBAL INITIATIVE OF ACADEMIC NETWORKS

09-DEC-2024 to 20-DEC-2024

SPONSORS

शिक्षा मंत्रालय
MINISTRY OF EDUCATION

Design | Integrate | Fabricate | Test

OVERVIEW

This course provides hands-on experience with next-generation design methodology and tools, RISC-V CPU design, and the semiconductor fabrication process. By participating, you will learn how large design teams work together to accomplish one of mankind's most remarkable accomplishments—turning sand into microchips with billions of transistors and teraflops of computing power. You will learn to use advanced design tools and methodologies powered by the open-source community before they are broadly adopted by the industry. You will learn RISC-V by building your own RISC-V CPU core!

After learning these skills and technologies, including Transaction-Level Verilog, the Makerchip IDE, and the Open Lane flow, you will be able to use them in an open-ended final project. Winning projects will be fabricated on the Skywater 130 nm process using Tiny Tapeout on Efabless's Chip Ignite multi-project wafer shuttle!

To suit participants from different backgrounds, the course is delivered in four modules, and participants may register for any or all modules based on interest and experience. See details on the registration page.

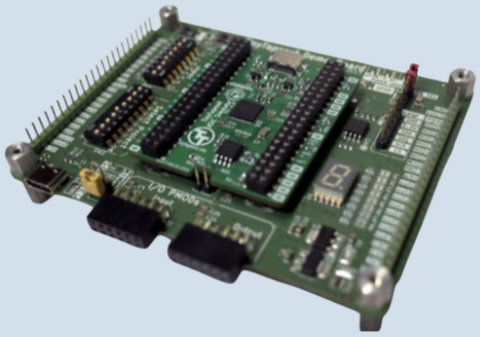
WHO CAN ATTEND ?

This course can be attended by both UG, PG students and research scholars who want to explore hardware design irrespective of their stream. It will also be helpful for faculty from academia and professionals from industry and R&D organizations. For outside participants, accomodation is available on payment basis.

PREREQUISITES

We welcome participants with diverse backgrounds, as no prior experience with hardware is necessary to excel in this course. All lab exercises use online tools. Participants MUST bring their own laptops every day.

TINY TAPEOUT



DATE OF EXAM: DEC 20, 2024

COURSE DETAILS

Module 1, Days 1-2: Digital Logic and CPUs

Introduction to Digital Logic

- **Topics:** Digital logic; sequential logic; pipelined logic; Tiny tapeout; FPGAs; TL-Verilog
- **Online tools:** Nand Game; Wokwi; Makerchip IDE; Compiler Explorer
- **Labs:** logic gates; counter circuit; Fibonacci series circuit; calculator circuit

CPUs

- **Topics**: compilers; assembly language
- **Online tools**: Compiler Explorer
- **Labs**: compilation; CPU operation

Module 2 (Days 3-5): Building a RISC-V CPU

Digital Logic

- **Topics:** Review of Module 1, Logic retiming, validity and clock gating
- **Online tools:** Makerchip IDE
- **Labs:** combinational circuit, pipeline, calculator with memory for Tiny Tapeout

RISC-V

- **Topics:** RISC-V ISA, application binary interface (ABI), CPUs
- **Online tools:** Compiler Explorer, WARP-V
- **Labs:** assembling/disassembling; programming/compilation, CPU simulation

Building a Single-Cycle RISC-V CPU

- **Topics:** caches and memories, CPU components
- **Labs:** next PC logic, fetch logic, decode logic, register read/ write, ALU

Pipelining the CPU

- **Topics:** waterfall diagrams, hazards
- **Labs:** simple pipelined CPU, register file bypass, branch redirect

Completing the CPU

- **Labs:** all instructions, loads/stores, jumps

Module 3 (Day 6): Semiconductor Industry Design Practices

Design Team Roles

- **Topics:** Roles, pre-silicon verification, post-silicon verification

EDA Tools

- **Topics:** Open Lane flow, logic synthesis, place &route, etc.

Future Methodologies

- **Topics:** hardware description languages, transaction-level design/verification, AI in EDA

Module 4 (Days 7-10): Open Projects

ATTENTION PLEASE! Selected projects will be fabricated using Tiny Tapeout

REGISTRATION DETAILS

CATEGORY	REGISTRATION FEE (including GST)
Research Scholars/ PG / UG (3rd year onwards) Students	₹1180
Faculty/Researchers from Academic/ Research Institutions	₹1180
Engineers from Industry and R&D Organizations	₹2360

You can pay directly to the following account or use a QR code for UPI payments. Once paid, please register yourself using the following link.

https://forms.gle/9zyBNMPo6EPtWsnS8

Account Holder Name	CEP, IIT BHUBANESWAR
Account No	**24282010001960**
Bank & Branch	Canara Bank, IIT Bhubaneswar,Argul Branch
IFSC Code	**CNRB0017282**
MICR Code	**752015014**

SCAN ME

CEP IIT BHUBANESWAR

234391134001960@cnrb

ACCOMODATION

Outstation participants can stay in our campus hostels on payment basis. If you need an accommodation, please fill out the form given in the link below.

https://forms.gle/fJAYA1syYmDpaBFn9