# Ayan Palchaudhuri

Email: ayanpalchaudhuri@gmail.com, ayan@iitbbs.ac.in

Website: sites.google.com/site/ayanpalchaudhuri

DBLP: dblp.org/pid/116/4755.html

ResearchGate: www.researchgate.net/profile/Ayan_Palchaudhuri

Google Scholar Profile: scholar.google.co.in/citations?user=qu4O9BsAAAAJ&hl=en

## Education

- Ph.D. in Electronics and Electrical Communication Engineering, Indian Institute of Technology Kharagpur, India.
- M.S. in Computer Science and Engineering, Indian Institute of Technology Kharagpur, India.
- B.Tech. in Electronics & Communication Engineering, The West Bengal University of Technology, (currently known as Maulana Abul Kalam Azad University of Technology), West Bengal, India.

## Research and Publications

### Research Interests

VLSI Architecture Design, FPGA Architectures, Hardware Description Language, Computer Arithmetic

### Peer Reviewed Journals (in reverse chronological order)

1. **A. Palchaudhuri**, D. Anand and A. S. Dhar, "FPGA fabric conscious architecture design and automation of speed-area efficient Margolus neighborhood based cellular automata with variegated scan path insertion", *Journal of Parallel and Distributed Computing (JPDC)* vol. 167, pp. 50-63. (2022)
2. **A. Palchaudhuri** and A. S. Dhar, "Speed-Area Optimized VLSI Architecture of Multi-bit Cellular Automaton Cell based Random Number Generator on FPGA with Testable Logic Support", *Journal of Parallel and Distributed Computing (JPDC)* vol. 151, pp. 13-23. (2021)
3. **A. Palchaudhuri**, S. Sharma and A. S. Dhar, "Design Automation for Tree based Nearest Neighborhood Aware Placement of High Speed Cellular Automata on FPGA with Scan Path Insertion", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 26, no. 4, pp. 31:1-31:34. (2021)
4. **A. Palchaudhuri** and A. S. Dhar, "Testable Architecture Design for Programmable Cellular Automata on FPGA Using Run-Time Dynamically Reconfigurable Look-Up Tables", *Journal of Electronic Testing, Theory and Applications (JETTA)*, vol. 36, no. 4, pp. 519-536. (2020)
5. **A. Palchaudhuri** and A. S. Dhar, "Fault Localization and Testability Approaches for FPGA Fabric Aware Canonic Signed Digit Recoding Implementations", *Journal of Electronic Testing, Theory and Applications (JETTA)*, vol. 35, no. 6, pp. 779-796. (2019)
6. **A. Palchaudhuri** and A. S. Dhar, "Design and automation of VLSI architectures for bidirectional scan based fault localization approach in FPGA fabric aware cellular automata topologies", *Journal of Parallel and Distributed Computing (special issue on Parallel Computing in Modelling and Simulation) (JPDC)*, vol. 130, pp. 110-125. (2019)
7. **A. Palchaudhuri** and A. S. Dhar, "Built-In Fault Localization Circuitry for High Performance FPGA Based Implementations", *Journal of Electronic Testing, Theory and Applications (JETTA)*, vol. 33, no. 4, pp. 529-537. (2017)
8. **A. Palchaudhuri**, A. A. Amresh and A. S. Dhar, "Efficient Automated Implementation of Testable Cellular Automata Based Pseudorandom Generator Circuits on FPGAs", *Journal of Cellular Automata (JCA)*, vol. 12, no. 3-4, pp. 217-247. (2017)
9. R. S. Chakraborty, I. Saha, **A. Palchaudhuri** and G. K. Naik, "Hardware Trojan Insertion by Direct Modification of FPGA Configuration Bitstream", IEEE Design & Test, vol. 30, no. 2, pp. 45-54. (2013)

**Conference Proceedings (in reverse chronological order)**

1. S. Adhikary and **A. Palchaudhuri**, "Fast Bit-Sliced VLSI Architectures on FPGA for Montgomery Domain Modular Inversion", $38^{th}$ *International Conference on VLSI Design (VLSID)*, Bengaluru, India, January 4-8, pp. 433-438. (2025)

2. S. Kumar and **A. Palchaudhuri**, "Leveraging Dual Output LUTs with Pipelining for Efficient BCD to Binary Converter on FPGA", $38^{th}$ *International Conference on VLSI Design (VLSID)*, Bengaluru, India, January 4-8, pp. 493-498. (2025)

3. S. Kumar and **A. Palchaudhuri**, "Exploring Efficient BCD to Binary Conversion Architecture Alternatives on FPGA", $31^{st}$ *IEEE International Conference on High Performance Computing, Data and Analytics (HiPC)* 2024 - Workshops, Bangalore, India, December 18-21, pp. 117-118. (2024)

4. **A. Palchaudhuri** and A. S. Dhar, "FPGA Specific Speed-Area Optimized Architectures of Arithmetic Cores with Scan Insertion for Carry Chain Based Multi-level Logic Implementation", $37^{th}$ *International Conference on VLSI Design (VLSID)*, Kolkata, India, pp. 617-622. (2024)

5. **A. Palchaudhuri** and A. S. Dhar, "Primitive Instantiation for Speed-Area Efficient Architecture Design of Cellular Automata based Mageto Logic on FPGA with Built-In Testability", $28^{th}$ *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Fayetteville, Arkansas, USA, pp. 207. (2020)

6. **A. Palchaudhuri**, S. Sharma and A. S. Dhar, "Placement Aware Design and Automation of High Speed Architectures for Tree-Structured Linear Cellular Automata on FPGAs with Scan Path Insertion", $28^{th}$ *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Seaside, California, USA, pp. 316. (2020)

7. **A. Palchaudhuri** and A. S. Dhar, "FPGA Fabric Conscious Design and Implementation of Speed-Area Efficient Signed Digit Add-Subtract Logic through Primitive Instantiation", $53^{rd}$ *Annual Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, USA, pp. 1555-1559. (2019)

8. **A. Palchaudhuri** and A. S. Dhar, "VLSI Architectures for Jacobi Symbol Computation", $32^{nd}$ *International Conference on VLSI Design*, New Delhi, India, pp. 335-340. (2019)

9. **A. Palchaudhuri** and A. S. Dhar, "Redundant Binary to Two's Complement Converter on FPGAs through Fabric Aware Scan Based Encoding Approach for Fault Localization Support", IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), $25^{th}$ Reconfigurable Architectures Workshop (RAW), Vancouver, British Columbia Canada, pp. 218-221. (2018)

10. **A. Palchaudhuri** and A. S. Dhar, "Fast Carry Chain based Architectures for Two's Complement to CSD Recoding on FPGAs", $14^{th}$ *International Symposium on Applied Reconfigurable Computing (ARC)*, Santorini, Greece, pp. 537-550. (2018)

11. **A. Palchaudhuri** and A. S. Dhar, "High Speed FPGA Fabric Aware CSD Recoding with Run-time Support for Fault Localization", $31^{st}$ *International Conference on VLSI Design*, Pune, India, pp. 186-191. (2018)

12. **A. Palchaudhuri** and A. S. Dhar, "Redundant Arithmetic Based High Speed Carry Free Hybrid Adders with Built-In Scan Chain on FPGAs", $24^{th}$ *IEEE International Conference on High Performance Computing (HiPC)*, Jaipur, India, pp. 104-113. (2017)

13. **A. Palchaudhuri** and A. S. Dhar, "Primitive Instantiation Based Fault Localization Circuitry for High Performance FPGA Designs", $21^{st}$ *International Symposium on VLSI Design and Test (VDAT)*, Roorkee, India, pp. 594-606. (2017)

14. **A. Palchaudhuri** and A. S. Dhar, "High Performance Bit-Sliced Pipelined Comparator Tree for FPGAs", $20^{th}$ *International Symposium on VLSI Design and Test (VDAT)*, Guwahati, India, pp. 1-6. (2016)

15. **A. Palchaudhuri** and A. S. Dhar, "Efficient Implementation of Scan Register Insertion on Integer Arithmetic Cores for FPGAs", $29^{th}$ *International Conference on VLSI Design*, Kolkata, India, pp. 433-438. (2016)

16. **A. Palchaudhuri**, R. S. Chakraborty and D. P. Sahoo, "Automated Design of High Performance Integer Arithmetic Cores on FPGA", $18^{th}$ Euromicro Conference on Digital System Design (DSD), Madeira, Portugal, pp. 322-329. (2015)

17. **A. Palchaudhuri**, R. S. Chakraborty, Md. Salman, S. Kardas and D. Mukhopadhyay, "Highly Compact Automated Implementation of Linear CA on FPGAs", *Cellular Automata - $11^{th}$ International Conference on Cellular Automata for Research and Industry (ACRI)*, Krakow, Poland. Published in Lecture Notes on Computer Science, Springer, vol. 8751, pp. 388-397. (2014)

18. S. Burman, **A. Palchaudhuri**, R. S. Chakraborty, D. Mukhopadhyay and P. Singh, "Effect of Malicious Hardware Logic on Circuit Reliability", $16^{th}$ *International Symposium on VLSI Design and Test (VDAT)*, Shibpur, India. Published in Lecture Notes on Computer Science, Springer, vol. 7373, pp. 190-197. (2012)

### Book

1. **A. Palchaudhuri** and R. S. Chakraborty, "High Performance Integer Arithmetic Circuit Design on FPGA-Architecture, Implementation and Design Automation," *Springer Series in Advanced Microelectronics*, ISBN 9788132225195 (print), 9788132225201 (ebook) (2016)

### Book Chapter

1. **A. Palchaudhuri** and R. S. Chakraborty, "A Fabric Component based Approach to the Architecture and Design Automation of High Performance Integer Arithmetic Circuits on FPGA", in M. Fakhfakh, E. Tlelo-Cuautle and P. Siarry (ed.), *Computational Intelligence in Electronic Design – Digital and Network Designs and Applications*, Springer (Switzerland), ISBN 978-3-319-20070-5 (print), 978-3-319-20071-2 (ebook) (2015)

### Patent

1. R. S. Chakraborty and **A. Palchaudhuri**, "Architecture and Design Automation of High Performance Large Adders and Counters on FPGA through Constrained Placement", International PCT application filed in April 2014 (Ref: PCT/IB2014/060372). Indian Patent filed in February 2014 (Ref: 179/KOL/2014).

## Competitions / Conferences

1. **[BEST POSTER AWARD] A. Palchaudhuri**, S. Sharma and A. S. Dhar, "FPGA Fabric Conscious High Speed Design and Scan Insertion through Efficient Logic Utilization", $12^{th}$ *Student Research Symposium (SRS) of the* $26^{th}$ *IEEE International Conference on High Performance Computing (HiPC), Data and Analytics*, Hyderabad, India. (2019)

2. **[BEST POSTER AWARD] A. Palchaudhuri** and R. S. Chakraborty, "High Performance Integer Arithmetic Circuit Design on Reconfigurable Computing Platforms", $7^{th}$ *Student Research Symposium (SRS) of the* $21^{st}$ *IEEE International Conference on High Performance Computing (HiPC)*, Goa, India. (2014)

3. **A. Palchaudhuri**, "FPGA Implementation of High Performance Testable Logic Insertion in Bit-Sliced Architecture Design", $28^{th}$ *IEEE Asian Test Symposium, Semi-Final of 2020 TTTC's E. J. McCluskey Doctoral Thesis Award*, Kolkata, India. (2019)

4. **A. Palchaudhuri** and A. S. Dhar, "FPGA Fabric Aware Design of VLSI Architectures", *PhD Forum of the* $30^{th}$ *International Conference on VLSI Design (VLSID)*, Hyderabad, India. (2017)

5. **A. Palchaudhuri** and R. S. Chakraborty, "Architecture and Design Automation of High Performance Arithmetic Architectures on FPGAs", *User/Designer Track of the* $28^{th}$ *International Conference on VLSI Design*, Bangalore, India. (2015)

## Project Experience

**Junior Project Assistant** Feb. 2011 – Sep. 2013

- "Hardware Security : Ensuring TRUST in Integrated Circuits" carried out in the Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur

**Project Experience** 28 Nov. 2011 – 18 Dec. 2011

- Worked for Centre for Artificial Intelligence and Robotics (CAIR), DRDO Bangalore, on Hardware Malware Vulnerabilities & Mitigation Techniques for FPGAs

## Course Information

**Teaching Courses at IIT Bhubaneswar**

- EC6L081: Architecture Design for Digital ICs
- EC6L066: Digital CMOS VLSI Design
- EC6L061: Architectural Design of VLSI Systems
- EC6L051: Mathematical Foundations of VLSI Systems
- EC6L053: Digital Integrated Circuit Design
- EC2L008: Introduction to Signal Processing
- EC6P057: Chip Design & Simulation Lab-II
- EC6P055: Chip Design & Simulation Lab-I
- EC2P001: Introduction to Electronics Laboratory
- EC6P054: Reconfigurable Computing Lab
- EE1P001: Electrical Technology Laboratory
- EE3P005: Measurement and Instrumentation Laboratory

**Teaching Courses at DA-IICT Gandhinagar**

- MC112: Computer Organization and Programming
- MC113: Computer Organization and Programming Lab
- IC121: Digital Logic and Computer Organization (Theory and Lab)

## Research Funding

1. Seed Grant IIT Bhubaneswar
    - Project Title: FPGA Fabric Conscious Architecture Design and Inclusion of Testability for High Performance Decimal Arithmetic in Human-centric Applications
    - PI: Dr. Ayan Palchaudhuri
    - Duration: 2 years ($20^{th}$ March 2024–$19^{th}$ March 2026)

## Positions of responsibility

- Served as Journal Reviewer for
    - Journal of Cryptographic Engineering (JCEN)
    - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
    - IEEE Transactions on Dependable and Secure Computing (TDSC)
    - Integration the VLSI Journal (Elsevier) **[Outstanding Contribution in Reviewing, August 2018]**
    - Future Generation Computing Systems (Elsevier)
    - Journal of The Institution of Engineers (India): Series B
- Invited to review a book chapter for the book on "Computational Intelligence in Electronic Design", Springer (Switzerland), M. Fakhfakh, E. Tlelo-Cuautle and P. Siarry (ed.)
- Invited to review papers for the following conferences:
    - IEEE TechSym 2016
    - $5^{th}$ International Symposium on Electronic System Design (ISED) 2014
    - $1^{st}$ International Conference on Intelligent Computing and Applications (ICICA) 2014

## Professional and Academic Honors

- Recipient of Science and Engineering Research Board (SERB) International Travel Support Grant, Department of Science and Technology, Government of India, for participating and presenting a research paper in $28^{th}$ ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, USA (23-Feb-2020 to 25-Feb-2020)
- Outstanding Contribution in Reviewing for Integration the VLSI Journal (Elsevier), August 2018
- Best Poster Award winner in the Student Research Symposium (SRS) of the IEEE International Conference on High Performance Computing (HiPC), in 2019 and 2014

## Professional Membership

IEEE, ACM