Dr. Akshay K

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Education

Program	Discipline	Institution	CGPA (Percentage)	Year of Completion
Accelerated Ph.D. (with MS)	Electrical Engineering	IIT Madras	9.76/10	2022
B.Tech	Electronics and Communication Engineering	NIT Calicut	9.28/10	2017
XIIth Std.	---	Placid Vidya Vihar (CBSE)	95.8/100	2013
Xth Std.	---	Chinmaya Vidyalaya (CBSE)	Full A^{+}	2011

Scholastic Achievements

- **Best Research Poster 2025 @ ISPEC, Gandhinagar**
- **AWSAR Award 2021**
  - Issued by the Department of Science and Technology, Govt. of India.
  - Awarded to 100 selected articles nationally "disseminating the research outputs of Ph.D. among the masses in an easy to understand and interesting format to a common man".
- **Institute Research Award 2021**
  - Issued by IIT Madras as a "recognition of the quality and quantity of research during Ph.D.".
  - First rank in the Department of Electrical Engineering, IIT Madras.
- **Prime Minister's Research Fellowship 2019**
  - Issued by the Ministry of Education, Govt. of India; The flagship Ph.D. fellowship that "seeks to attract the country's best talent into research".
  - The first recipient in the Department of Electrical Engineering, IIT Madras.
- **Best Major Project Award, NIT Calicut 2017**
  - Issued by NIT Calicut as a "recognition of the quality and quantity of work done as a part of B.Tech project".
- Secured **5**th rank in the outgoing B.Tech batch of the Department of Electronics and Communication Engineering, NIT Calicut.

Professional Experience

- **Assistant Professor** **Oct 2023 – Present**
  - **School of Electrical and Computer Sciences, Indian Institute of Technology Bhubaneswar**
  - Currently supervising three Ph.D scholars, teaching one theory course and two labs.
- **Director and Co-Founder** **Apr 2024 - Present**
  - **Nano Semic Pvt. Ltd.:** Company based on semiconductor products and services.
- **Visiting Assistant Professor** **May 2023 – Oct 2023**
  - **School of Electrical Sciences, Indian Institute of Technology Bhubaneswar**
- **Senior Engineer NAND Device, Technology Development** **Aug 2022 - Mar 2023**
  - **Micron Technology, Inc.**: Responsible for the design and optimization of *biasing schemes* for next-generation non-volatile 3D-NAND flash memory transistor arrays.
- **Post-Doctoral Fellow** **May 2022 - July 2022**
  - **IIT Madras**: Appointed for submitting the Ph.D. thesis within 5 years.
  - Proposed a novel drift layer design method for increasing the breakdown voltage of SiC-Power MOSFETs by up to 68 % with just 6% increase in specific on-resistance. This work was done in collaboration with Prof. Anant Agarwal's group at Ohio State University.
  - Mentored a Ph.D. scholar by reviewing his work and suggesting directions to explore.

Research Projects

Funding agency	Amount (in lakhs INR)	Start Date	End Date	Title	PI/Co-PI
iVP Semi	$100k USD	Apr 2025	Apr 2027	Design and Development of Si MOSFETs for eV application	Yes
ANRF	72	March 2025	March 2028	Design and Characterization of SiC Trench MOSFETs for Next Generation Power Electronic Applications	Yes
IIT Bhubaneswar	20	Oct 2025	Oct 2027	Simulation, Design and Feasibility Investigation of Superjunction based Power Devices in 4H-SiC Material	Yes
INUP-i2i	In-kind			Investigation of Al2O3/SiO2 Interface on Silicon Carbide Substrate to study the feasibility of Charge Sheet Super Junction	Yes

Teaching Experience

New Courses Introduced in Curriculum June 2024

IIT Bhubaneswar

M.Tech in STCD

- Power Semiconductor Devices and Technology
- MOS Device Modeling and Characterization
- Advanced Memory Devices

Theory Courses and Labs Conducted May 2023 – Present

IIT Bhubaneswar

- Power Semiconductor Devices and Technology to M.Tech and PhD.
- VLSI Design theory and lab course to 6th semester B.Tech ECE students.
- Microprocessors and Microcontrollers Theory and Lab for 5th semester B.Tech ECE students.
- Electrical Technology Lab for 1st semester B.Tech students for several disciplines.

Online and Offline Talks 2017 – 2022

NIT Calicut

- Several offline talks, webinars, and freshman orientation sessions for ECE students of NIT Calicut (a sample recording can be found here.)
- Consistently received a rating of > 4.5 (out of 5) from the audience (e.g. a webinar feedback form)

Teaching Assistant Jul 2018 – Apr 2022

IIT Madras

- Post Graduate courses: Power Semiconductor Devices, MOS Device Modeling, Semiconductor Device Modeling.
- Under Graduate course: Digital Systems.
- Responsible for holding biweekly discussion sessions, preparing question papers and their solutions, invigilation, and evaluation.

Teaching Assistant Jul 2020 – Apr 2022

NIT Calicut

- As a part of Prime Minister's Research Fellowship.
- Post Graduate courses: MOS Device Modeling, Semiconductor Device Modeling
- Responsible for preparing question papers, and assignments and deciding the marking scheme.

Technical Talk Series Jul 2020 – Apr 2022

NIT Calicut

- Initiated a "Talk of the Month" technical talk series by and for the students at NIT Calicut under the banner of IEEE Electron Devices Society Student Branch.
- Delivered 2 talks and organized several talks.

Online and Offline Talks 2017 – 2022

NIT Calicut

- Several offline talks, webinars, and freshman orientation sessions for ECE students of NIT Calicut (a sample recording can be found here.)

Administrative Responsibilities

UG Coordinator of Department of ECE October 2024 – Present
IIT Bhubaneswar

- *Instrumental in curriculum revision for B.Tech ECE as per NEP guidelines.*

Professor in Charge (IDEA Lab) July 2024 – Present
IIT Bhubaneswar

- *Secured research grants and consultancy projects worth > 1.5 crores and procured high end work stations and power device characterization equipments.*

Professor in Charge (Micro Fabrication and Characterization Lab) May 2024 – Present
IIT Bhubaneswar

Faculty Coordinator for Placements and Internships (ECE) May 2024 – Present
IIT Bhubaneswar

- *Instrumental in enabling 6-month internship for graduate students.*
- *Instrumental in increasing number of core-companies coming to campus for placements/internships e.g. Micron, Synopsys, Texas Instruments, Qualcomm, Rambus*

SES Aesthetics Committee Member May 2024 – Present
IIT Bhubaneswar

Research Collaborations

SiC D-MOSFET Design

Aug 2021 – Ongoing
Ohio State University

- In collaboration with Prof. Anant Agarwal of Ohio State University.
- Developed novel strategies for the design of floating field rings (TCAD-based) and drift layer (analytical method based on Lagrange Multipliers).
- Designed for breakdown voltage > 700 V. Manuscript under preparation.

Thermal Modeling of β-Ga_2O_3 Transistor

Feb 2020 – Dec 2020
Purdue University

- In collaboration with Prof. M. A. Alam of Purdue University.
- Derived a physical equation for estimating the effective thermal resistivity of a multi-layer stack of materials. This equation reveals why the layers closer to the heat source contribute more to effective thermal resistivity than farther away layers.
- Awaiting experimental data from the Purdue team for model validation.

SiC Schottky Diode Design

Aug 2018 – Jan 2019
DRDO

- In collaboration with the Research and Innovation Centre (RIC) of DRDO for in-house manufacturing of SiC power devices as a part of the 'Make in India' initiative.
- Designed the doping, geometry, and masks for 700 V breakdown voltage and 25 A on-current.

MOS_2 Schottky Diode Study

May– Jul 2018
IIT Delhi

- In collaboration with Prof. Rajendra Singh of IIT Delhi. who fabricated MOS_2 Schottky barrier diodes
- TCAD simulator calibration and parameter extraction of doping, mobility, and surface charge.

- Studied current distribution contour and showed that contact length can be reduced by > 95 %. Presented at IEEE ICEE.

Research Internships

8 kV Silicon Thyristor Design and Manufacturing
Aug – Sept 2021

Ruttonsha International Rectifiers Limited

- Received hands-on training in manufacturing processes such as diffusion, oxidation, etching, photolithography, passivation, packaging, and electrical characterization of high-power Si devices.
- Designed an 8 kV thyristor and prepared the key technological milestones towards manufacturing it.

Silicon LDMOS Modeling
Jan – May 2021

IISc Bangalore

- Under the guidance of Dr. Mayank Shrivasthava
- Derived closed-form physics-based equation for the breakdown voltage of LDMOS devices using ionization integral approach. TCAD validation and manuscript preparation under progress.
- Analyzed the filamentation-related failure under ESD conditions.

4-H SiC VD-MOSFET Design
May – Jul 2016

IIT Madras

- Under the guidance of Dr. Shreepad Karmalkar
- Worked on 4-H SiC VD-MOSFET drift layer design using charge sheet super junction concept
- A novel algorithm for optimizing spacing between the floating field rings for edge termination has been tried and compared with existing approaches.

Power Device Simulation
May – Jul 2015

NIT Calicut

- Under the guidance of Mr. Jaikumar M G
- Learned and successfully mastered Softwares: ATLAS (TCAD simulation), and MATLAB (numerical calculation and plotting).
- Simulated high voltage Si diodes, MOSFETs, and IGBTs to understand device physics and operation.

Journal Articles

[1] P. Singh, S.Karmalkar, and **K. Akshay**, “Humidity and Ring Spacing Variation Tolerant Design of a SiC Power MOSFET Using Mirrored Floating Field Rings”, Microelectronics Journal, vol. 158, p. 106611, Apr. 2025.

[2] P. Singh, S.Karmalkar, and **K. Akshay**, “Improved Short Circuit Performance of Silicon Carbide VD-MOSFETs Using an Additional P+ Implant”, Microelectronics Reliability, vol. 166, pp.115614, Apr. 2025.

[3] S. Mahalik, **K. Akshay**, S. Dey, "A 2D-MoS_2 -Based Thin-Film Transistor for Trace-Level SO_2 Monitoring," *IEEE Transactions on Electron Devices*, vol. 72, no. 1, pp. 390-396, Jan. 2025.

[4] Anuvindh R, S. Mahalik, A. Roy, **K. Akshay**, S. Dey, "Conductance Spectroscopy: A Novel Technique for Ultra Selective Chemical Detection," *IEEE Sensors Journal*, vol. 24, no. 24, pp. 40417 – 40422, Nov. 2024.

[5] **K. Akshay** and S. Karmalkar, **“**Optimum Aspect Ratio of Superjunction Pillars Considering Charge Imbalance,” *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp.1798-1803, Mar. 2021

[6] **K. Akshay** and S. Karmalkar, "Improved Theoretical Minimum of the Specific On-Resistance of a Superjunction," *Semicond. Sci. Technol.*, vol. 36, no. 1, p. 015021, Dec. 2020.

[7] **K. Akshay** and S. Karmalkar, "Note Clarifying "Charge Sheet Super Junction in 4H-Silicon Carbide: Practicability, Modeling and Design"," *IEEE J. Electron Devices Soc*., vol. 8, pp.1315-1316, Oct. 2020.

[8] **K. Akshay** and S. Karmalkar, "Charge Sheet Super Junction in 4H-Silicon Carbide: Practicability, Modeling and Design," *IEEE J. Electron Devices Soc*., vol. 8, pp. 1129 – 1137, Sep. 2020.

[9] **K. Akshay** and S. Karmalkar, "Quick Design of a Superjunction Considering Charge Imbalance Due to Process Variations," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3024 3029, Aug. 2020.

[10] M. G. Jaikumar, **K. Akshay**, and S. Karmalkar, "An algorithm to design floating field rings in SiC and Si power diodes and MOSFETs," *Solid-State Electron*., vol.156, pp.73-78, Jun. 2019.

Conference Proceedings and Poster Presentations

[1] K. J. Swadhin, P. Chiranjeebi, **K.Akshay**, P.V. Satyam, "Investigation of Al2O3/SiO2 Interface Charge for the Feasibility Study of Charge Sheet Super Junction", in *Proc. IEEE Electron Devices Technology & Manufacturing Conference*, 2025.

[2] M. Mrinmoy, K. Prathamesh, and **K. Akshay**, "TCAD based Study of String Current Variability in 3D NAND Flash Memory", in *Proc. 38th IEEE International Conference on VLSI Design*, 2025.

[3] P. Singh, **K. Akshay**, H.L.R. Maddi, A. Agarwal, S. Karmalkar, "Design of the Drift Layer of 0.6–1.7 kV Power Silicon Carbide MOSFETs for Enhanced Short Circuit Withstand Time," *in Proc. IEEE EDTM,* 2023.

[4] **K. Akshay**, M. G. Jaikumar and S. Karmalkar, "Charge Sheet Super Junction in 4H-Silicon Carbide," in *Proc. IEEE EDTM*, 2020.

[5] **K. Akshay**, R. P. Parvathy and B. Bhuvan, "Enhancement of Full Well Capacity of a Pinned Photodiode," *IWPSD*, 2019.

[6] **K. Akshay**, M. Moun, R. Singh and S. Karmalkar, "TCAD Simulation of the Measured I-V Behaviour of Schottky Contacts on Exfoliated MoS_2 Flakes," *IEEE ICEE*, 2018.

[7] **K. Akshay**, R. P. Parvathy and B. Bhuvan, "System Level Design of a Novel CMOS Image Sensor with High Dynamic Range and Fill Factor," in *Proc. IEEE TENCON*, 2019.

[8] **K. Akshay**, R. P. Parvathy and B. Bhuvan, "Analytical Modeling of Response Time and Full Well Capacity of a Pinned Photo Diode," in *Proc. IEEE DTIS*, Italy, 2018.

[9] **K. Akshay**, R. P. Parvathy and B.Bhuvan, "Optimum length of a pinned photodiode," in *Proc.IEEE EDSSC*, Hsinchu, 2017.

Relevant Course Projects

Integrated Circuit Design of a High Dynamic Range CMOS Image Sensor Jul 2016 – Apr 2017

NIT Calicut

Major Project

- Under the guidance of Dr. Bhuvan. B
- Derived closed-form solution for the optimum length, full well capacity, and response time of a pinned photodiode and validated with TCAD simulations. Presented in four conferences.
- Proposed a novel logarithmic pixel with a high fill factor, dynamic range, and speed.

Device Simulation of Power Devices and Hardware Implementation of Smart DTMF Communication
Dec 2015 – Apr 2016

Mini Project ***NIT Calicut***

- Under the guidance of Dr. Jaikumar M G.
- Simulated avalanche breakdown of power semiconductor devices like diode, U-MOSFET, and IGBT.
- Using DTMF communication, four modes of operation were implemented to do home automation, surveillance, and encrypted message transfer.

Technical Society Activities

Founder Chairman of IEEE Electron Devices Society Student Branch
2015-2017

NIT Calicut

- One of the 18 student chapters in Asia.
- Organized 3 distinguished lectures for 240^{+} B. Tech students and 3 school workshops on basic electronics for 500^{+} students.
- Procured grants and profitably managed an annual budget of up to 1 Lakh. Led a team of 6 executive members.
- Initiated and organized 9 biweekly student lectures to cultivate research interest among students.
- Delivered over 6 seminars and webinars and consistently received above 9/10 audience feedback scores for the overall quality.

Senior Executive at Department Student Association
2016-2017

NIT Calicut

- Organized 5 technical and non-technical events.
- Co-designed and coordinated the setting up of electronics stall during the college technical festival.

Softwares

- **Simulation**: Expert in Silvaco ATLAS and MATLAB. Novice in Sentaurus**,** Virtuoso Cadence, LT Spice, Labcenter electronics Proteus, and Arduino IDE.
- **Plotting, Text, and Video Editors**: JMP, Origin, Latex, Microsoft Office, Adobe Premiere Pro

Extra-Curricular Activities

Arts : Co-directed, edited, and acted in two short films. Received three years of training to play Tabla.
Sports : Regular cardiovascular exercising and weight training. Played as a center-back (defender) in the school football team
Travel : Traveling (group and solo) for sightseeing, self-reflection, and to experience new cultures and food.